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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,176	02/23/2004	Kun-Hong Chen	250122-1270	8529
24504	7590	03/09/2005	EXAMINER	
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 100 GALLERIA PARKWAY, NW STE 1750 ATLANTA, GA 30339-5948			VU, QUANG D	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/785,176

Applicant(s)

CHEN, KUN-HONG

Examiner

Quang D. Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 December 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of group II (claims 9-17) in the reply filed on 12/02/04 is acknowledged.

Claim Objections

Claim 14 is objected to because of the following informalities: There is no antecedent basis for the claimed limitation "the metal layer" as claimed in the claim 14. Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 9, 12, 13, 14, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,297,519 to Fujikawa et al.

Regarding claim 9, Fujikawa et al. (figure 4B) teach an interconnect structure, comprising:

a substrate (1);

a dielectric layer (4) disposed on the substrate (1);

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a first metal layer (22) disposed in the dielectric layer (4), having a first (portion of the top surface) and second (portion of the bottom surface) end;

a second metal layer (35b) disposed on the dielectric layer (4), wherein the second metal layer (35b) is isolated from the first metal layer (22) by the dielectric layer (4); and

a plurality of conductive plugs (portions [35b] in the contact holes [25b]) disposed in the dielectric layer (4) and on the first end (portion of the top surface) of the first metal layer (22) to electrically connect the second metal layer (35b).

Regarding claim 12, Fujikawa et al. teach the number of conductive plugs is 2, which is in the range of the claimed invention.

Regarding claim 13, Fujikawa et al. teach the conductive plugs (portions [35b] in the contact holes [25b]) disposed on the first end (portion of the top surface) of the first metal layer (22) electrically connect one end of the second metal layer (35b).

Regarding claim 14, Fujikawa et al. (figure 4B) teach an interconnect structure, comprising:

a substrate (1);

a dielectric layer (4) disposed on the substrate (1);

a first metal layer (22) disposed in the dielectric layer (4), having a first (portion of the bottom surface) and second (portion of the top surface) end;

a second metal layer (35b) disposed on the dielectric layer (4); and

a plurality of plugs (portions [35b] in the contact holes [25b]) disposed on the first end (portion of the bottom surface) of the first metal layer (22), wherein the plug (portion [35b] in the

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contact hole [25b]) farther from the first end (portion of the bottom surface) of the first metal layer (22) is conductive and electrically connects the second metal layer (35b).

Regarding claim 16, Fujikawa et al. teach the number of plugs is 2, which is in the range of the claimed invention.

Regarding claim 17, Fujikawa et al. teach the conductive plug (portion [35b] in the contact hole [25b]) electrically connects one end of the second metal layer (35b).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 10, 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujikawa et al. in view of US Patent No. 6,737,305 to Lee et al.

Regarding claim 10, Fujikawa et al. differ from the claimed invention by not showing the substrate is a TFT-array substrate for an LCD panel. However, Lee et al. teach the LCD panel comprises a TFT array substrate (column 1, lines 37-39). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Lee et al. into the device taught by Fujikawa et al. in order to improve the property and the reliability of the liquid crystal display (LCD) panel.

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Regarding claim 11, the combined device shows the first metal layer (Fujikawa et al.; 22) and the second metal layer (Fujikawa et al.; 35b) are a gate metal layer and a source/drain metal layer of a TFT array respectively.

Regarding claim 15, the disclosures of Fujikawa et al. and Lin et al. are discussed as applied to claims 14, 16 and 17 above.

The combined device differs from the claimed invention by not showing the substrate is a TFT-array substrate for an LCD panel. However, Lee et al. teach the LCD panel comprises a TFT array substrate (column 1, lines 37-39). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Lee et al. into the device taught by Fujikawa et al. and Lin et al. in order to improve the property and the reliability of the liquid crystal display (LCD) panel.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
February 23, 2005



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800